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THERMAL AND RADIATION STABILITY OF THIN-FILM CERMET RESISTIVE ELEMENTS

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August 1969

**GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland**

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John L. Tarpley

ABSTRACT

Recent laboratory experiments indicate that cermet thin-film resistors consisting of a mixture of 80 percent chromium and 20 percent silicon monoxide can be fabricated to a high sheet resistance of 4500 ohms per square with pronounced thermal and radiation stability. Cermet films produced in this study had a thermal stability of < 1 ppm/ $^{\circ}$ C from -50 $^{\circ}$ C to +175 $^{\circ}$ C and a radiation stability of $\leq 1\%$ variance in absolute resistance for fluences up to 1×10^{15} e/cm² at a 1.5 Mev energy level. Cermet resistor fabrication techniques are shown to be physically compatible with silicon semiconductor integrated circuit (IC) technology. Cermet thin-film resistors offer a stable, wide-range alternative to the inherent instabilities and relatively narrow range of values of present-day silicon resistors.

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THERMAL AND RADIATION STABILITY OF THIN-FILM CERMET RESISTIVE ELEMENTS

INTRODUCTION

From recent studies that project into future usage of integrated circuits (IC's) it is now apparent that new and improved resistor elements for silicon monolithic integrated circuits must be produced if IC's are to achieve the level of high performance demanded by rigorous deep space applications. The traditional silicon resistor in IC's, consisting of a diffused layer and reverse-bias junction, does not meet the basic requirements of IC's for space applications such as: low temperature coefficients, precision and wide range of resistance values, and minimal parasitic capacitance. However, cermet thin-film resistors have shown that they closely approach these critical requirements and in addition, bring to the IC a resistor element with controlled thermal and radiation stability.

Early work on cermets, reported in 1959 by IBM (1) was not very encouraging. However, with the concerted efforts of a number of investigators (2 and 3), considerable improvement has been achieved lately in terms of thermal stability, fabrication control, and understanding the physical nature and electrical properties of cermet. The potential combination of the metal-dielectric components in cermets are numerous; many systems have already been studied. They include: Ni-Cr, Ta-Ta₂O₅, TaSi-CrSi, Pt-WO₃, Pt-Ta₂O₅, Au-WO₃, and Au-Ta₂O₅. Mixtures of Ta, Si, Cr, and Al₂O₃ have also been under investigation (4).

Recently, the Cr-SiO cermet thin-film resistor has been favored because of its excellent stability under both thermal stress and humidity, as well as stability in storage (2 and 6). A temperature coefficient of resistance (TCR) of less than 1 ppm/°C has been obtained in a useful range of sheet resistance (up to 4500 ohms/square). Thus, the high sheet resistance values attainable in cermet elements afford considerable reduction in the area density requirements of the resistor portion of an IC.

This report discusses some of the physical controls attainable in cermets and the electrical properties attainable in thin-film cermet elements when employed apart from IC devices. Some of the properties attainable when cermet elements are built into IC's are also discussed.

Texas Instruments (TI), under NASA contract, fabricated the cermet devices studied in this program and performed the thermal tests. Details of their work

are discussed in Reference 5. The radiation performance evaluation was carried out at the NASA-Goddard radiation facility and is reported here.

CERMET CHARACTERISTICS AND PROPERTIES

Material Composition

The cermet charge material studied is a powder mixture of 80 percent by weight chromium and 20 percent by weight silicon monoxide which represents 77.1 atomic percent chromium and 22.9 mole percent silicon monoxide. The chromium is a 300 mesh powder containing as the dominant impurity copper in concentrations of 1 to 10 ppm. The silicon monoxide is Kemet Select Grade (#10 mesh vacuum baked) mechanically pulverized fine powder. The two powders were thoroughly mixed in the ratio mentioned above.

Fabrication

An oil diffusion, liquid nitrogen trapped, vacuum system was used for cermet evaporation with system pressure varying between 9×10^{-6} and 2×10^{-7} torr. Resistor deposition was carried out by downward evaporation of the Cr-SiO powder mixture contained in a resistance heated boat arranged as in Figure 1. This configuration had a source-to-substrate distance of six inches, with target slices positioned face-upward on an insulated stainless steel table, heated from below by quartz incandescent tubes. An externally operated manual shutter was located between the source and target.

Critical Steps in Charge Deposition

Factors affecting a good vacuum deposition, such as maintaining absolute cleanliness within the bell-jar, were absolutely essential to controlling the physical and electrical properties of the evaporated cermet. Outgassing of target slices was achieved by heating to 450°C for 30 minutes prior to deposition. Generally, the pressure transient was smaller when the powder charge was pre-heated before a deposition run. Figure 2 is typical of the sequence followed during the cermet deposition.

To eliminate possible contact resistance errors, sheet resistance of the deposited film was monitored by a four-terminal method. The choice of monitor materials and temperature were controlled so as to duplicate the conditions of deposition on the target-slices. The monitor itself was fabricated by first caving-tronning a standard hall bar sample from chemically polished silicon which was further refined by light chemical etching. This was followed by oxidation of the silicon bar to 5000\AA , then Si_3N_4 deposition to 1000\AA by the reaction of silane and

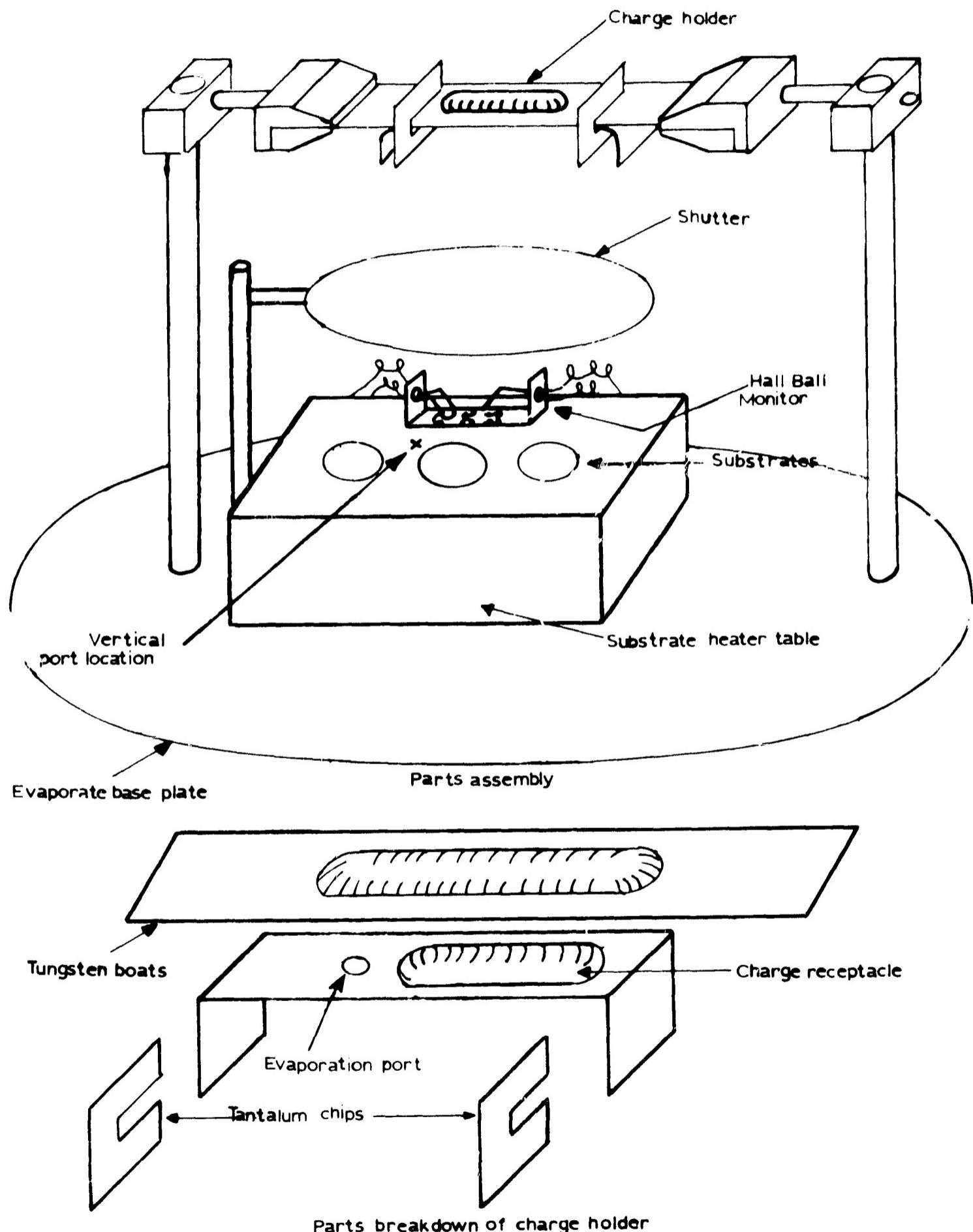


Figure 1. Evaporator Components Arranged for Cr-SiO Cermet Deposition

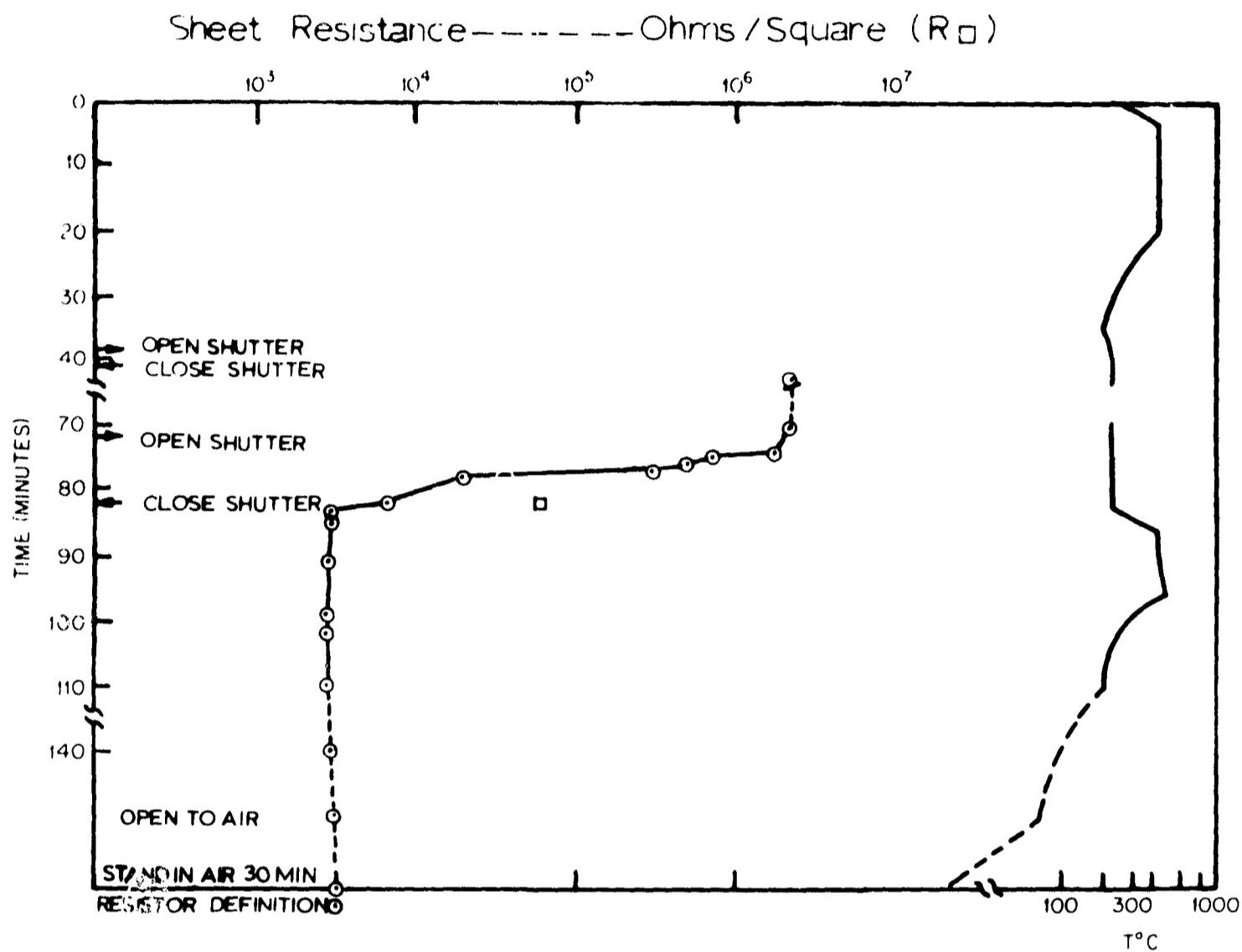


Figure 2. Deposition Sequence

ammonia in a hydrogen diluent at 850°C . Evaporated aluminum contacts were then applied. The monitor was placed in a spring contact fixture for cermet deposition as shown in Figure 1.

The question of deposition uniformity was resolved by adding microscope slides to an early run, and determining film thickness values by interferometer measurements. These measurements showed a thickness variation from 417\AA to 590\AA with a system accuracy of $\pm 100\text{\AA}$.

Resistor Profile

Three types of resistor patterns were included in this study. Two of the patterns were made to evaluate resolution capability and the effects of resistor aspect ratio and contact resistance. The third pattern, adopted for circuit construction (see Figure 3) permitted the use of the reverse aluminum process which defined cermet strips to dimensions of 0.4 mil wide and 0.4 mil separation.

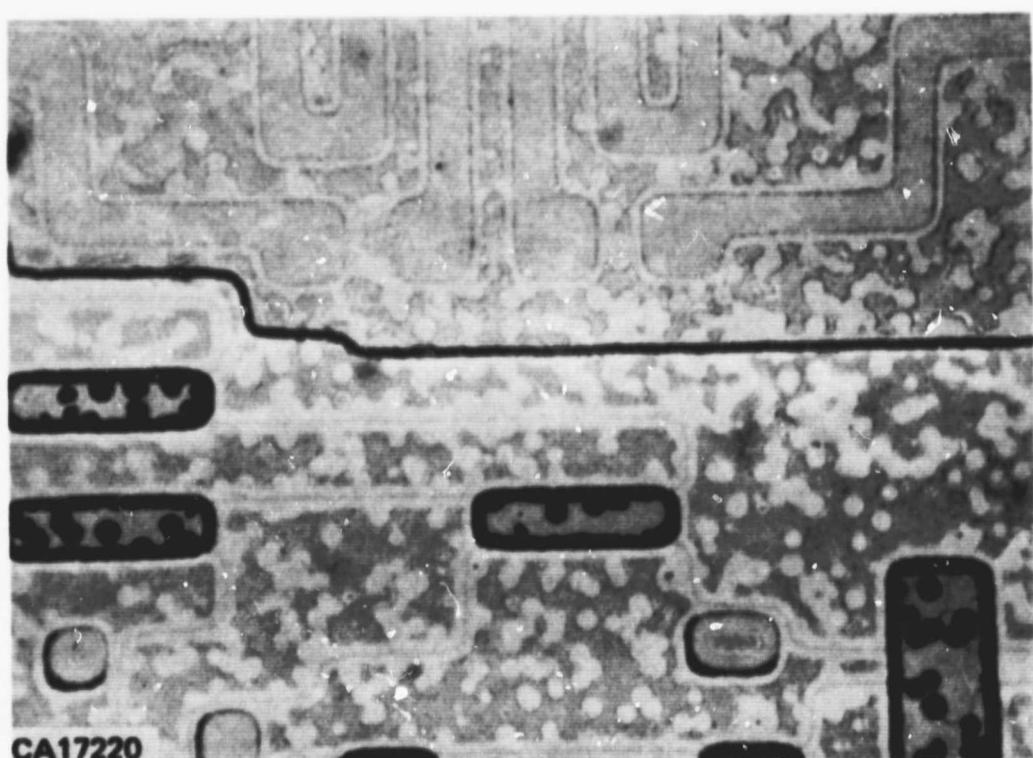


Figure 3. Cermet Patterns

The final arrangement of the cermet resistor sections was an array of six discretely tapped resistors on a common silicon chip. The chip was mounted on a TO-5 low profile header and enclosed in a kovar case.

Temperature Coefficient of Resistance (TCR)

Cermet resistors produced show a TCR of less than 1 ppm/ $^{\circ}$ C in the temperature range between -50 $^{\circ}$ C and +175 $^{\circ}$ C for a sheet resistance of 4400 ohms/square. Resistance versus temperature curves for typical devices are shown in Figures 4a and 4b. They are characterized by a small negative coefficient which is attributed partly to film composition, partly to annealing, and partly to chromium corrosion.

The temperature characteristics of cermet thin-film resistors were also evaluated by Braun and Lood (6). They show a tracking coefficient (deviation in the ratio of two resistors as a function of temperature) for a cermet to be \pm 1 ppm/ $^{\circ}$ C from -150 $^{\circ}$ C to +150 $^{\circ}$ C.

Thermal Stress

Thermal stress behavior in Cr-SiO cermet resistive films have been studied by a number of investigators (1 through 4) with varying results. For this program, a controlled thermal stress analysis was conducted on 10 discrete cermet resistor elements that had been fabricated in the manner described earlier. The data corroborate previous findings in showing a high degree of thermal stress stability in the film.

The 10 cermet resistors underwent a thermal stress at 175 $^{\circ}$ C for 168 hours. To approximate a circuit function, the devices received a continuous dc load current of about 10 microamperes. Instability of resistance was within measurement accuracy of \pm 0.5% for this one-week test. To further evaluate their temperature response, six of the ten units were kept under thermal stress for an additional 168 hours at an increased load current of up to 70 microamperes. These samples continued to show no detectable change in resistance. The test data were taken by a direct x-y plot of current vs voltage for both positive and negative voltages up to 3.5 volts. Figure 5 shows a typical trace of the relationship between applied voltage and load current; it is linear and without measurable thermal effects.

In another study (6), a flash-evaporated Cr-SiO cermet mixture was evaluated. That study showed uniform drift in the direction of increasing resistance of approximately one percent per 1000 hours for storage at 200 $^{\circ}$ C and 0.25 percent per 1000 hours for storage at 150 $^{\circ}$ C. This small change was

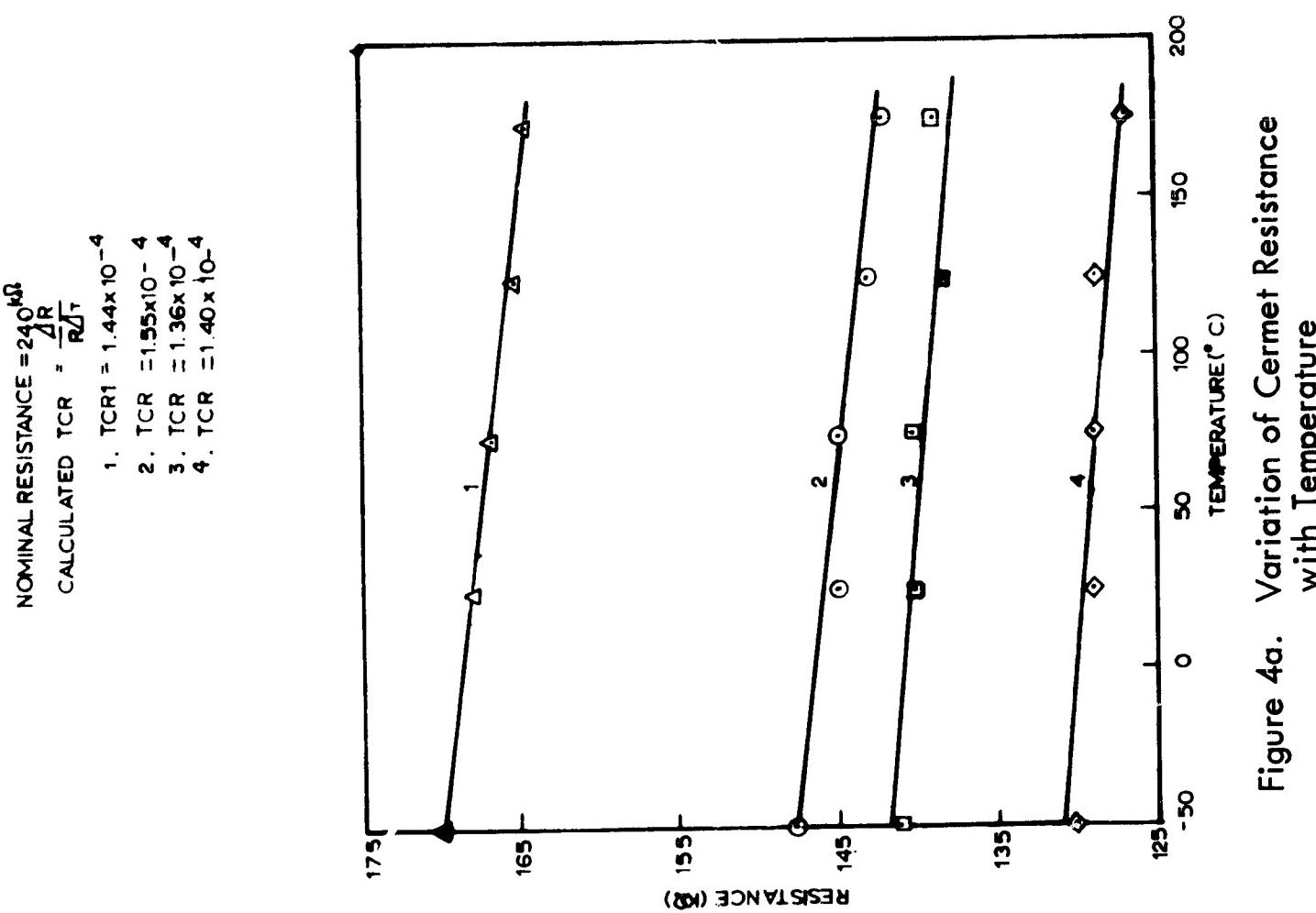


Figure 4a. Variation of Cermet Resistance with Temperature

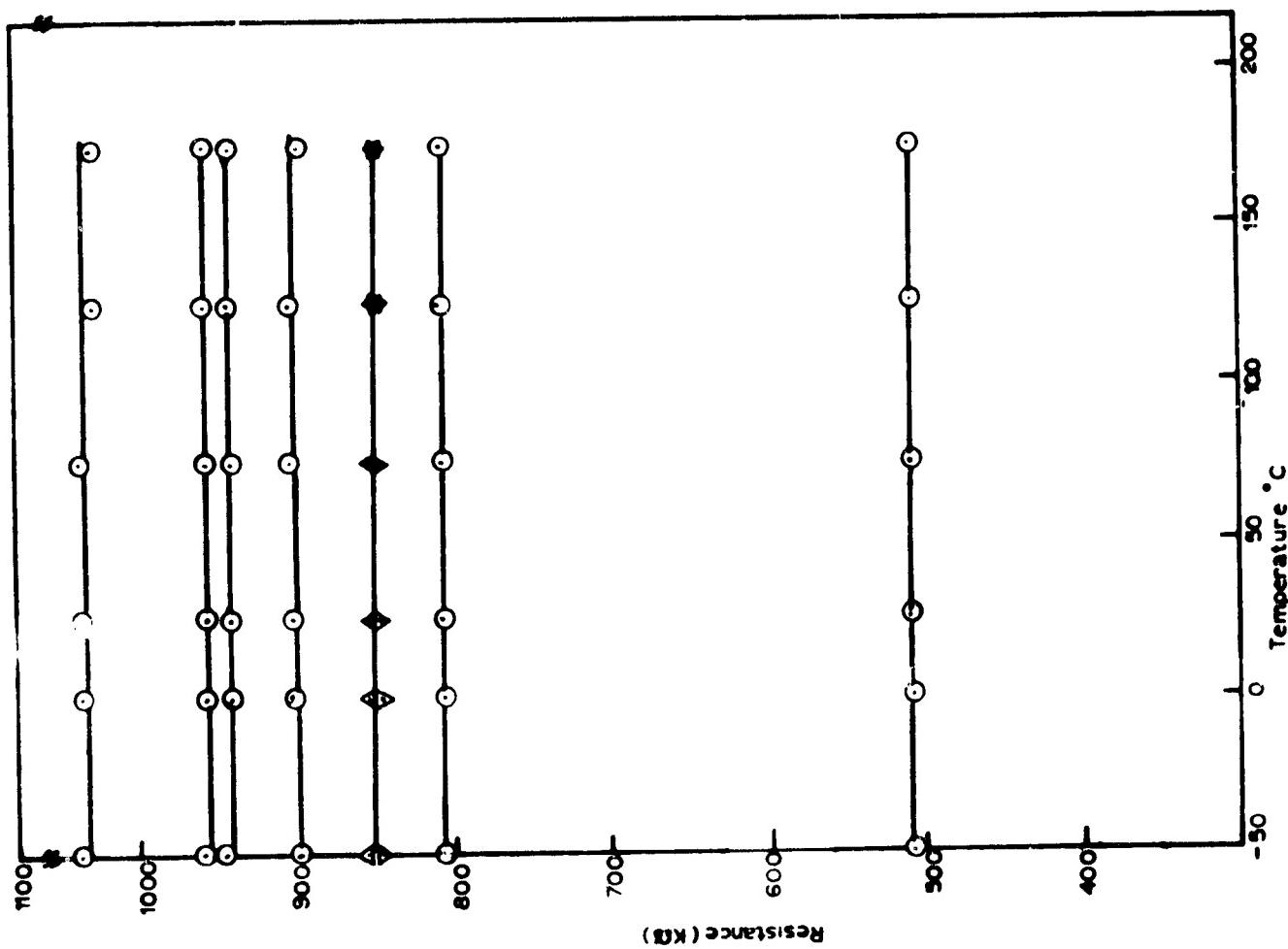


Figure 4b. Stable Temperature Response of Cermet Resistors

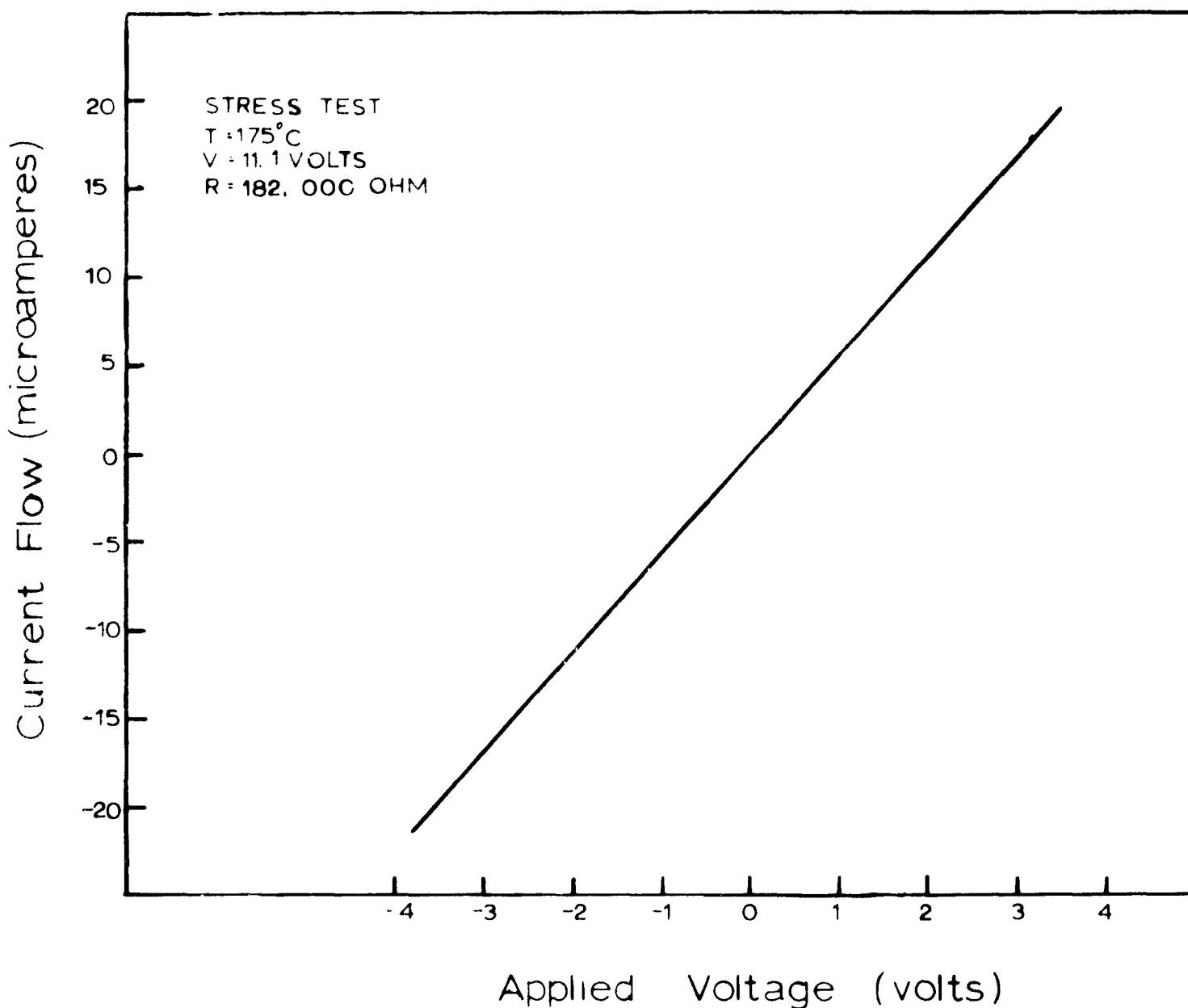


Figure 5. Stress Test Stability

attributed to oxidation of the chromium. Stable characteristics were also observed in unprotected (uncased) resistor elements exposed directly to a temperature of 60°C and a relative humidity of 95 percent for 500 hours.

Radiation Stress

It has been shown that ceramic insulating materials such as Al_2O_3 , SiC , TiO_2 , BeO , and MgO have excellent radiation resistance under severe radiation bombardment of greater than $1 \times 10^{20} (\text{nVo})t$ (7). It is then conceivable that a "semi-insulating" material such as Cr-SiO (Cermet) might also exhibit good radiation resistance because of its ceramic constituent.

To test for radiation stability in cermets, a test lot of 24 cermet resistor elements were subjected to an intense radiation sequence of fluence levels up to

1×10^{15} e/cm² at an energy level of 1.5 Mev. These 24 resistors were a representative sample of the devices fabricated as previously described.

All resistors were loaded with 10 microamperes of dc current while being irradiated to simulate a typical circuit function. A Dymec Data Acquisition System, having an accuracy of ± 0.15 percent, recorded the absolute resistance values before, during, and after irradiation at programmed intervals.

Excursions in resistance values during irradiation were within one percent of initial values, and in each case, showed a trend toward slightly decreasing values with higher fluence, as depicted in Figure 6. The slight drop-off in resistance from irradiation was probably due to radiation annealing. Annealing effects in some cermet mixtures are expected to cause recrystallization and bridging of isolated island groups within the mixture (3), reflecting a downward trend in resistance. The precise composition of the cermet mixture also is expected to heavily influence the extent of radiation annealing.

Very little is reported in the literature on radiation effects on cermets. One study, conducted by IBM for the United States Army (8), was an evaluation of a 50/50 Cr-SiO mixture sandwiched between a layer of SiO on each side. This study revealed radiation-induced leakage current in the resistor elements, indicating air ionization effects. Effects on the absolute resistance values were not reported.

CERMET RESISTORS IN INTEGRATED CIRCUITS (IC)

Compatibility with IC's

To show the compatibility of cermet thin-films with IC's, employing a layered insulator of silicon nitride (Si_3N_4) on silicon dioxide (SiO_2), a simple design of a binary counter circuit was chosen for fabrication. The topology of this circuit was such that no p-diffused region was used for the sole purpose of tunneling under a metal lead. Where tunnels were required, already existing drains or sources were extended to provide the tunnel, thus minimizing load capacitance. A schematic diagram of the test circuit is given in Figures 7a and 7b.

The layout of the cermet load resistors was arranged so that a single set of masks provided circuits having four different nominal values of resistance; this was accomplished by simply ball-bonding to appropriate taps on a resistor stripe. The active elements in this circuit were metal nitride-oxide semiconductor field effect transistors (MNOSFET) with conductance values ultimately determined by speed and "saturation" voltage requirements. Speed was limited primarily by

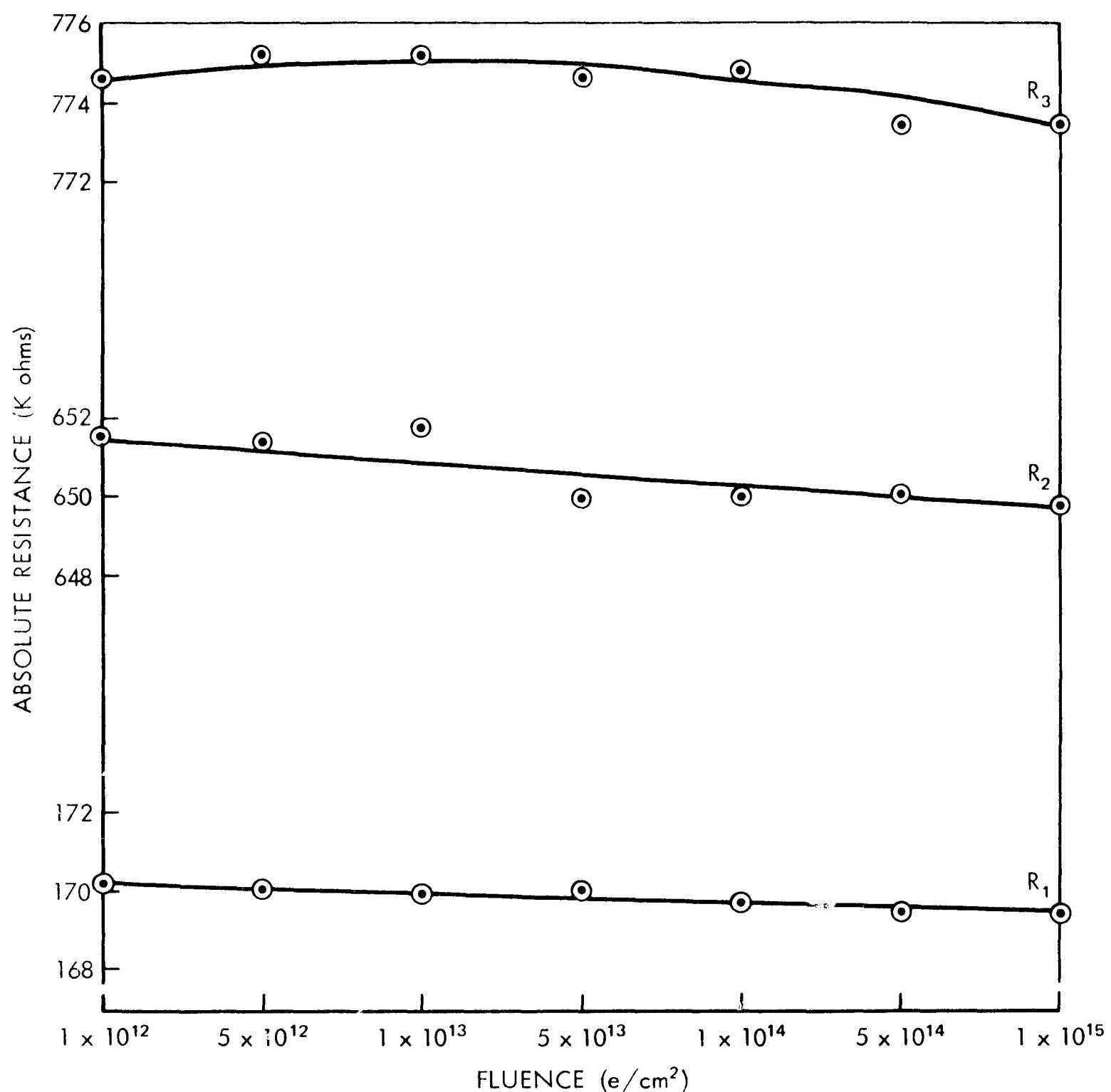


Figure 6. Typical Stability Curves for Cermet Resistors During Irradiation (Radiation Energy - 1.5 Mev)

the time constant set by the product of the load resistor (Cermet) and the MNOSFET input capacitance. In MNOSFET's, a decrease in the channel length lowers capacitance while raising conductance, so the minimum length that is consistent with present technology, 0.2 mils (after lateral diffusion), was used. A decrease in channel width lowers both input capacitance and conductance of the device, while raising the saturation voltage.

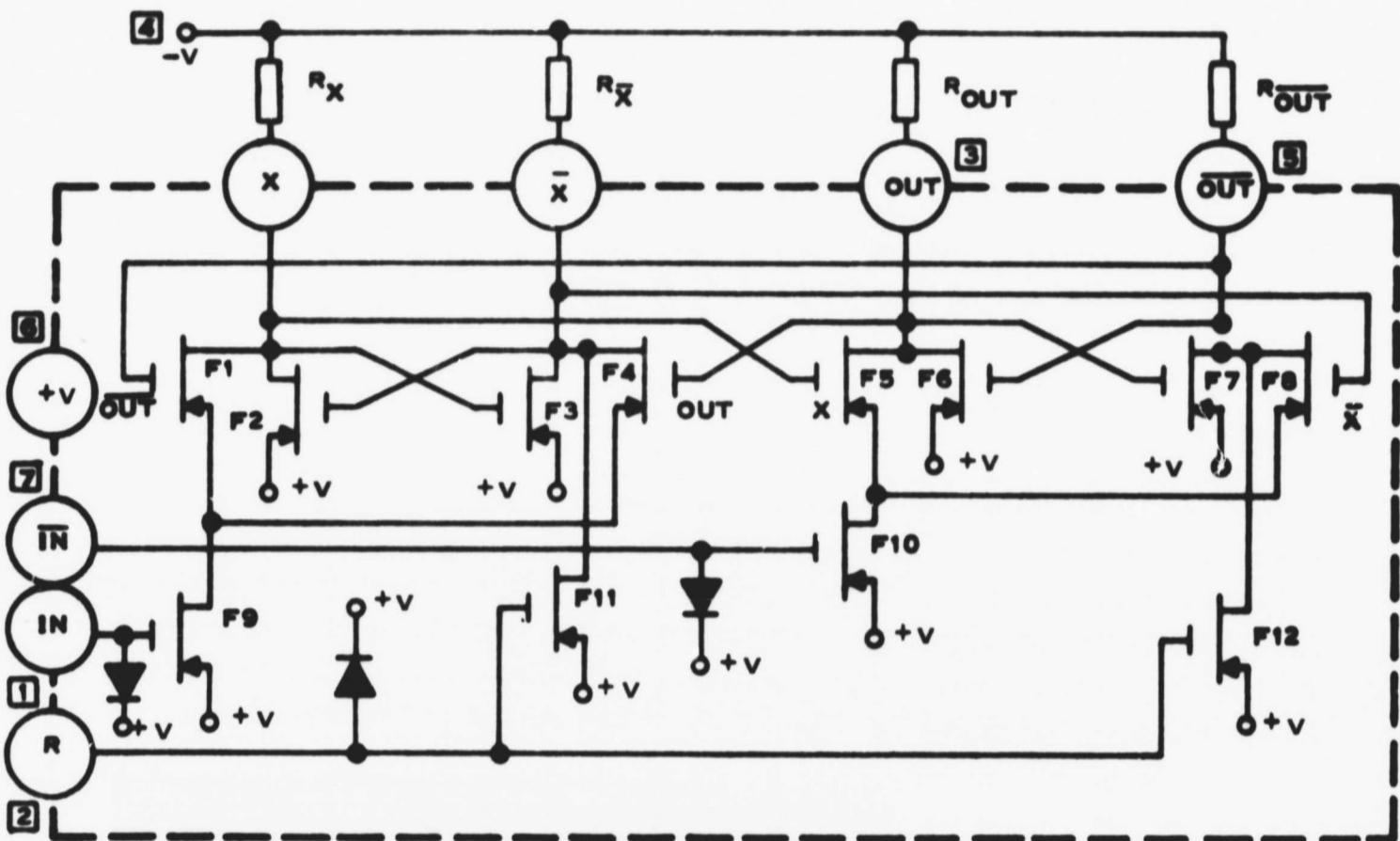


Figure 7a. Schematic Binary Counter Circuit

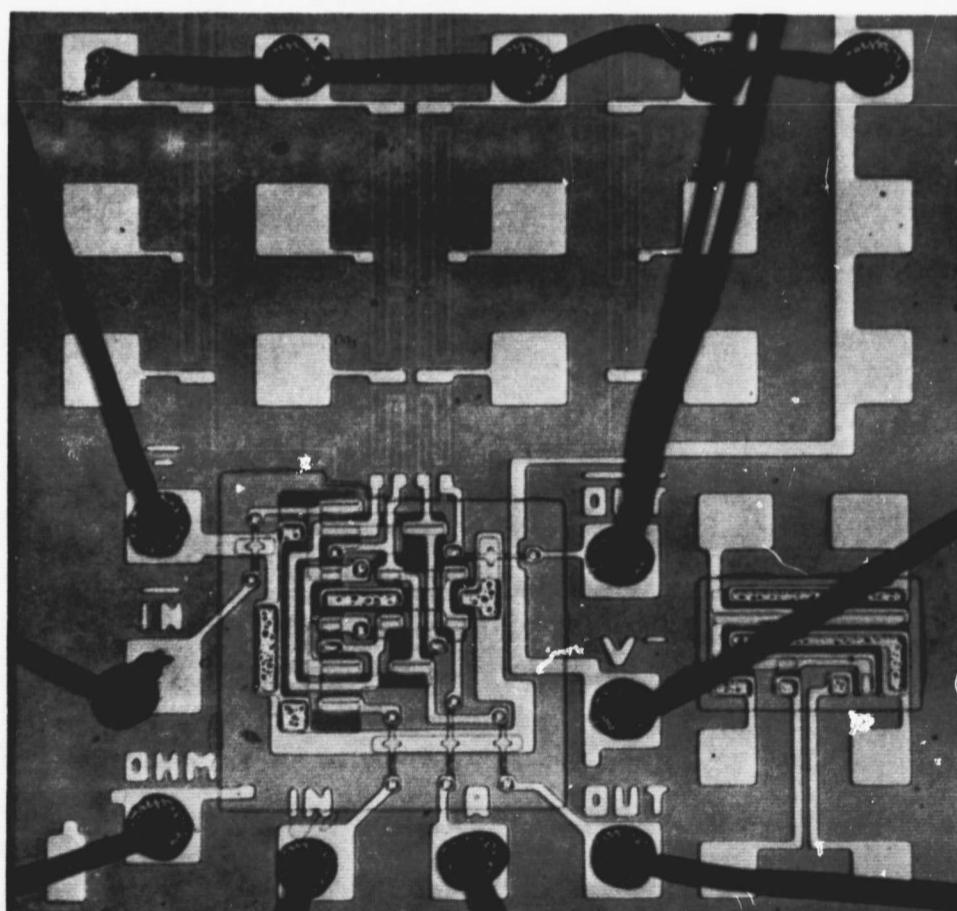


Figure 7b. Ball-Bonded Binary Counter Chip Configuration

Circuit Performance

Speed was the circuit parameter optimized in this design and it far exceeded the 256 kc specified level. For any given value of load resistance, the circuit made the binary division at frequencies up to five times greater than the specified minimum frequency of 246 kc. Thus, an operational advantage was gained because stray capacitance in the monolithic IC was minimized with the cermet film.

Radiation Stress

Six binary counter circuits were irradiated at an energy level of 1.5 Mev. A 1kHz square wave signal was applied to the counter input while the output pulse waveform was monitored by a Tektronix Type 585A Oscilloscope throughout a radiation exposure sequence. Figure 8 shows typical waveforms for both input and output connections. Degradation in the binary circuit performance due to radiation was reflected by distortion of the output pulse waveform.

FREQUENCY = 1 kHz
HORIZONTAL = 500 μ sec/cm
VERTICAL = 10 V/cm

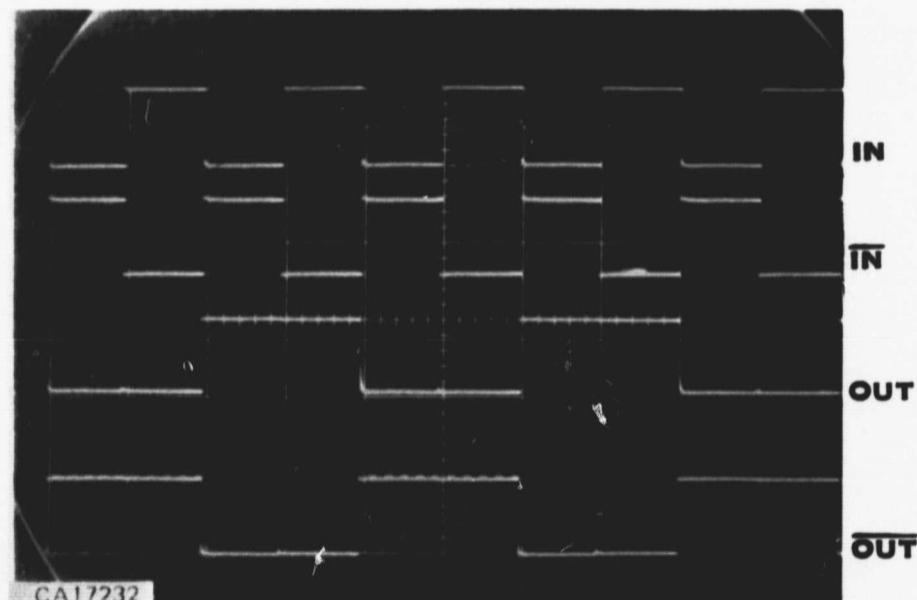


Figure 8. Typical Input-Output Waveforms for Binary Circuit Tests

Three of the six test devices had their gate threshold bias voltage (V_{TH}) adjusted as required to maintain an undistorted wave output pulse for each fluence level. Results from this radiation exposure indicated a minimum gate voltage shift for the individual devices at fluence levels up to 1×10^{12} e/cm². Between fluence levels of 1×10^{12} and 1×10^{13} e/cm², the gate threshold shifts were gradual and ranged from 1.83 to 4.64 volts for the three devices. Exposures beyond 1×10^{13} e/cm² showed rather abrupt shifts in gate threshold voltages, the largest overall shift being 20.9 volts. Figure 9 is a graphic description of the shifts in gate voltage versus fluence.

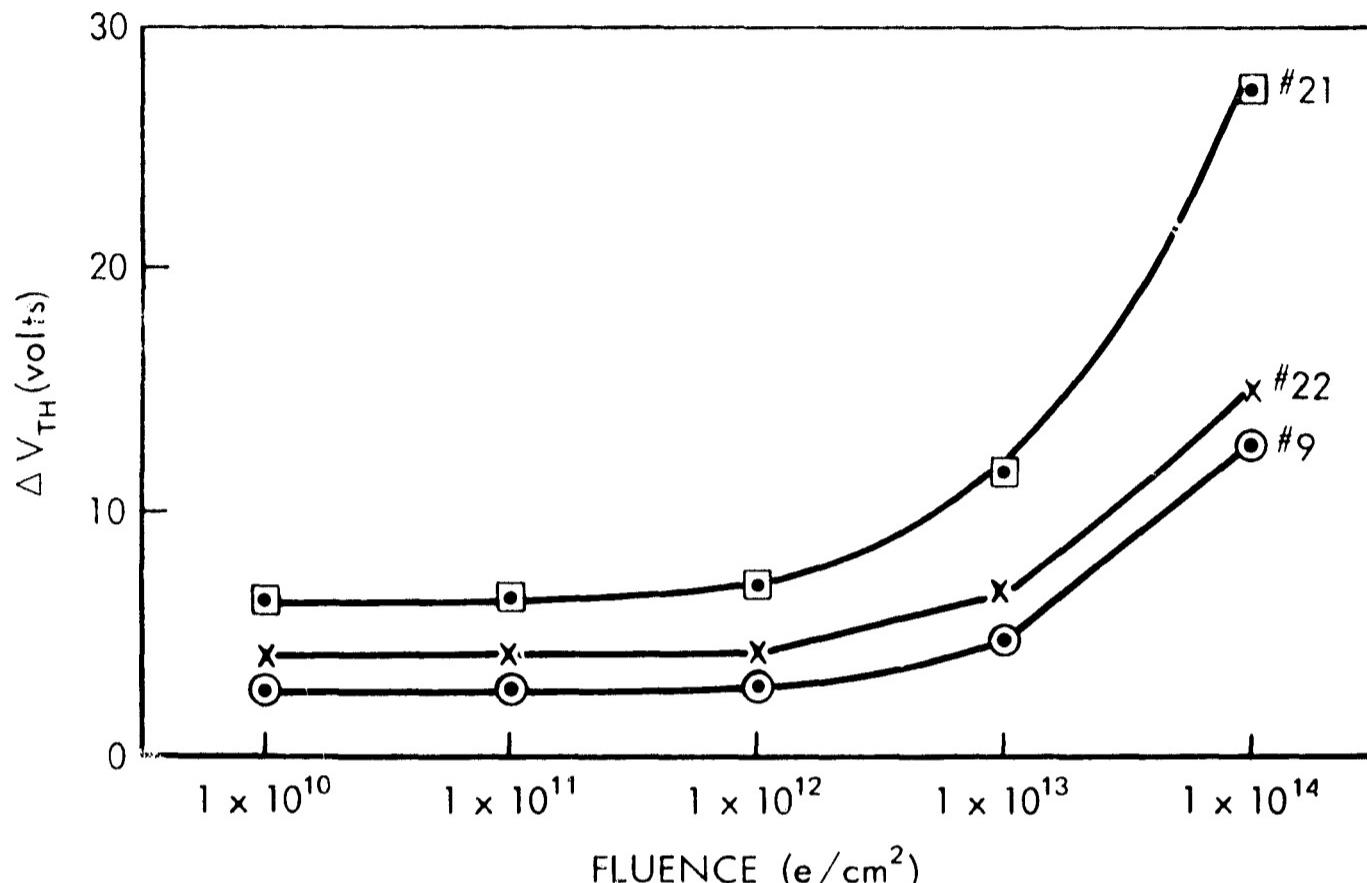


Figure 9. Threshold Voltage Shift in Binary Circuit vs Fluence

On three separate binary IC devices, the gate bias was set initially at -10 volts and kept constant at this level throughout the irradiation sequence. Again, a 1 kHz square wave signal was fed to the circuit input and the output waveform was continuously monitored.

Very little distortion of the output pulse was detected for radiation exposures up to $1 \times 10^{13} e/cm^2$. However, for radiation exposures between fluence levels of $1 \times 10^{13} e/cm^2$ and $1 \times 10^{14} e/cm^2$, the output pulse became noticeably distorted. Subsequent gate threshold voltage measurements following the radiation exposure at $1 \times 10^{14} e/cm^3$ showed that voltages of -13.6V, -14.5V, and -17.4V were required to restore the output pulses to normal. These post-radiation voltage levels approximate those of circuits with serial numbers 9 and 22 reported initially in this section for the continuously varying gate bias with fluence. The close agreement between the final threshold levels shows that the level of bias applied during irradiation had little apparent effect on the degree of radiation damage incurred.

The "damage mechanism" of ionizing radiation on insulated gate field effect transistors has been thoroughly investigated by the Radio Corporation of America (9) for NASA. The overall conclusion was that a buildup of trapped charge in the insulator is the cause of the radiation damage.

CONCLUSIONS

Cermet thin-film resistors have shown distinct performance advantages in the areas of thermal stability and low parasitic capacitance. Cermet deposited on silicon chips retains the desirable properties of an all-silicon IC device, such as controlled dimensions in microcircuit configurations plus good definition by photolithography. Cermet resistors show good radiation resistance, a property essential to preventing wide load level shifts in IC's under radiation bombardment. Cermet elements, when exposed to an intense radiation field, fluence up to 1×10^{15} e/cm², 1.5 Mev energy, showed less than a 1.0 percent change in absolute resistance. These features give cermet thin-film resistors a distinct advantage in performance characteristics over most silicon resistors, especially for spacecraft electronics operating in high radiation flux areas.

It is recognized that to build cermet resistors into monolithic IC's is more costly (about twice) than to build an all-silicon monolithic circuit because of the added processing steps. Cermet's closely circumscribed performance properties, however, could easily justify the increased cost under circuit conditions that demand close resistor tolerance (one percent) and functional stability in a severe space environment.

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REFERENCES

1. IBM, Federal Systems Division: "Thin-Film Circuit Functions," First Quarterly Progress Report, Contract No. DA36-039-SC-84547, Kingston, New York (U) AD232959
2. Glange, R., Holmwood, R. A., and Herd, S. R.: "Resistivity and Structure of Cr-SiO Cermet Films," J. Vac. Sc. Techn. vol. 4, no. 4, 1967, p. 163
3. Schaible, P. M., Overmeyer, J. C., and Glang, R.: "Load-Life Tests of Cr-SiO Cermet Thin-Film Resistors," Phys. of Failure in Electronics, vol. 5, Reliability Series, eds: Shilliday and Vaccaro
4. Motorola, Inc., Semiconductor Products Division: "Thin-Film RC Networks for Silicon Integrated Circuits," First Quarterly Report, Contract No. DA28-043 AMC-02212 (e), Phoenix, Arizona, AD647385, January 1967
5. Texas Instruments, Inc.: "Development of Silicon Nitride and Cermet Resistors For Use In A Binary Counter, Metal Insulator Field Effect Transistor Circuit," Final Report, Contract No. NAS5-10307, Dallas, Texas, 1 December 1966 - 31 May 1968
6. Braun, L., and Lood, D. E.: "Precision Thin-Film Cermet Resistors for Integrated Circuits," Proc. IEEE, vol. 54, no. 1521, Nov. 1966
7. Kircher, J. F., and Bowman, R. E.: "Effects of Radiation on Materials and Components," Reinhold, New York, 1964, pp. 42-43
8. IBM, Electronic Systems Center: "Study of Effect of High-Intensity Pulsed Nuclear Radiation on Electronic Parts and Materials (SCORRE)," First Annual Interim Report, Contract DA28-043-AMC-00212(E) DA Project No. 5901.21.700.01, Owego, New York
9. RCA: "The Interrelation of Process Techniques and Space Radiation Effects in Metal-Insulator-Semiconductor Structures," Final Report, Contract No. NAS5-10177, Princeton, New Jersey, 21 April 1966 - 31 July 1967